MEMORY ADDRESSING OF RANGE BLOCKS IN FRACTAL CODING

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to digital image processing and more specifically the compression of digital images by fractal coding.

Discussion of the Related Art

Fractal coding consists of searching, in a digital image, similar image portions to reduce the image volume by only, for the blocks considered as similar, coding a single block and identifying the other similar blocks by a reference to the first block.

Fig. 1 illustrates in a simplified view a digital image I in which a search window SW must be coded by fractal compression. The window is divided into blocks of same dimension, here B1, B2, ..., B5, ..., B9 of 32 by 32 pixels, search window SW being of 34 by 34 pixels. Blocks B1 to B9 overlap or cover one another in both directions. In practice, a search window of greater dimension is used, for example, 64 by 64 pixels. To simplify, the present invention will be described in relation with an example of a search window of 34 by 34 pixels. It however applies whatever the number of pixels of the search window and of the blocks.

The search for the similar blocks is performed with respect to a reference block also called range block RB of dimensions smaller than those of blocks B1 to B9. To enable comparison, blocks B1 to B9 are sub-sampled to obtain so-called domain blocks DB of same size as range block RB.

Fig. 2 illustrates this sub-sampling by a transformation of blocks Bi into domain blocks DBi. Each domain block contains values corresponding to the average pixel group values of the corresponding entire block.

The similarities between blocks RB and DB are not searched for identities only. It is also searched whether each domain block corresponds to the range block after given transformations. These transformations are called isometries and respectively correspond to a symmetry with respect to the vertical axis, a symmetry with respect to the horizontal axis, a 180° rotation, a symmetry of axis Y=X, a 270° rotation, a 90° rotation, and a symmetry of axis Y=-X.

The fractal image coding or compression technique is described, for example, in work "Fractal image compression: Theory and application to digital images" by Yuval Fisher, published by Springer Verlag, New-York, 1995. Another example of a fractal image compression algorithm is described in article "Design of an ASIC architecture for high speed fractal image compression" by Ancarani De Gloria and Olivieri Stazzone, published in IEEE "International ASIC conference", September 1996.

Those skilled in the art can also refer to French patent application 2,775,812.

To enable comparing domain blocks with the range block, the range block and its seven isometries must conventionally be stored in distinct memory areas.

Summary of the invention

The present invention aims at reducing the necessary memory space in a digital image fractal coding system.

The present invention more specifically aims at reducing the storage space necessary to the range block isometries.

To achieve these and other objects, the present invention provides a method for storing values of a range block and of seven isometries used in a fractal image compression method, consisting of using four memory areas of identical sizes in which are respectively stored the identity, and three first isometries corresponding to the isometries of symmetry with respect to the vertical axis, of 270° rotation, and of 90° rotation.

The present invention also provides a method for reading from memory areas in which each memory area is addressed in a first direction for the reading of the stored values to obtain the identity and the first three isometries, and in the reverse direction for the reading of the four other isometries of symmetry with respect to the horizontal axis, of 180° rotation, of symmetry with respect to a first diagonal, and of symmetry with respect to the second diagonal.

The present invention also provides a fractal image compression method using a range block and seven isometries of this block, including the steps of:

- memorizing the respective values of the pixels of the range block and of only three of its isometries; and
- addressing the corresponding memory areas in read mode in one direction or in the reverse direction according to the desired isometry.

According to an embodiment of the present invention, two isometries of the range block are stored in a same memory area.

The present invention also provides a circuit for addressing a memory of storage of an image data range block intended to be used in a fractal image compression method, including means for addressing each of four areas of said memory in a first direction and in the reverse direction.

The foregoing objects, features and advantages of the present invention will be discussed in detail in the following

non-limiting description of specific embodiments in connection with the accompanying drawings.

Brief Description of the Drawings

Figs. 1 and 2, previously described, illustrate the fractal image compression to which the present invention applies;

Fig. 3 illustrates the different isometries of a range block of a digital image in fractal coding according to an example of four by four pixels; and

Fig. 4 shows the architecture of a memory according to the present invention intended for the coding of the reference isometries in a fractal coding method.

Detailed Description

Same elements have been designated with same references in the different drawings. For clarity, only those elements and those method steps which are necessary to the understanding of the present invention have been shown in the drawings and will be described hereafter. In particular, the different calculations and processings upstream and downstream of the storages and of the reading of the range blocks have not been detailed and are no object of the present invention. Further, the sequencing of the processings of loading and unloading of the range blocks depends on the application and is no object of the present invention either.

Fig. 3 very schematically shows the seven possible isometries in a fractal image coding for a range block 1 of four by four pixels. The choice of the number of 16 pixels for the range block is arbitrary. The present invention applies whatever the number of pixels of the range blocks, provided that the blocks are square. In particular, most often, these blocks are blocks of eight by eight pixels, their size depending on the size of the obtained sub-sampled blocks (DBi, Fig. 2).

Reference block 1 is taken arbitrarily as the identity block, that is, in the case where pixels P1 to P16 of range block 1 correspond in values and arrangements to the pixels of the domain block being compared. In Fig. 3, the pixels of the range

block have been numbered as P1 to P16 and arranged line by line from left to right from the bottom of the block in the position of the drawing.

A first isometry 2 corresponds to a symmetry with respect to vertical axis Y centered in the middle of the range block. If a domain block corresponds to the arrangement shown in isometry 2 of Fig. 3, it will be considered that it is possible to transmit it in the form of the number of range block 1, associated with the parameter defining the isometry of vertical axis.

A second isometry 3 corresponds to a symmetry with respect to horizontal axis X centered in the middle of the reference image.

A third isometry 4 corresponds to a symmetry of axis Y=X. This amounts to a symmetry with respect to diagonal D_{XY}.

A fourth isometry 5 corresponds to a 180° rotation of the range block.

A fifth isometry 6 corresponds to a 270° rotation.

A sixth isometry 7 corresponds to a 90° rotation.

A seventh isometry 8 corresponds to a symmetry of axis Y=-X, that is, a reflection with respect to diagonal D_{-XY}.

A feature of the present invention is to only use four memory areas having a size corresponding to the size of the range block to store all the isometries necessary to the comparison.

Another feature of the present invention is to provide a reading of the isometries in reverse directions so that each memory area actually contains two isometries of the range block.

Fig. 4 illustrates, in a simplified view to be compared to that of Fig. 3, four memory areas M1, M2, M3, and M4 storing range block 1 shown in Fig. 3 and its isometries.

According to the present invention, a first memory area M1 contains arrangements 1 and 3, that is, the identity and the symmetry with respect to the horizontal axis.

A second memory area M2 contains isometries 2 and 4, that is, the symmetry with respect to the vertical axis and the 180° rotation.

A third memory area M3 contains isometries 5 and 6, that is, the symmetry of axis Y=X and the 270° rotation.

A fourth memory area M4 contains isometries 7 and 8, that is, the 90° rotation and the symmetry of axis Y=-X.

As appears from Fig. 4, to obtain the different isometries, it is enough to organize the reading from the corresponding memory area, once from top to bottom, then, from bottom to top.

Such a reading is easily implementable by means of a memory addressing circuit, parameterized according to the type of isometry with which the current domain block is desired to be compared.

An advantage of the present invention is that it divides by two the memory space necessary for the storage of the range blocks and of their respective isometries.

Another advantage of the present invention is that it results in no complexity of the memory selectors. The only counterpart is a read-adapted programming of memory areas M1 to M4 containing the range block isometries.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, although the present invention has been described in reference to isometries of range blocks of 4 x 4 pixels, it applies to any square range block and its isometries.

Further, the present invention more generally applies to any image processing method requiring storage of image block isometries, similar to those used in a fractal compression.

Moreover, the practical implementation of the circuits necessary to the implementation of the present invention and the control signals of addressing of the different memory areas are within the abilities of those skilled in the art based on the function indications given hereabove.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be

within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is: